

The listing of claims will replace all prior versions and listings of claims in the application:

**Listing of Claims**

1. (Currently Amended) A method of fabricating a contact of a semiconductor device, comprising:
  - patterning an interlayer dielectric of the semiconductor device to form a contact hole that exposes a silicon-based region of a first impurity type;
  - doping the exposed silicon-based region with a gas containing an element of the first impurity type under a chamber pressure of from about  $6 \times 10^{-2}$  to about  $6 \times 10^{-4}$  Torr; and
  - forming a contact plug in the contact hole.
2. (Original) The method of Claim 1, wherein the first impurity type is an n-type.
3. (Original) The method of Claim 1, wherein the gas containing an element of the first impurity type comprises AsH<sub>3</sub> and/or PH<sub>3</sub>.
4. (Original) The method of Claim 1, wherein the contact plug comprises doped polysilicon.
5. (Original) The method of Claim 4, wherein the doped polysilicon is doped with an element of the first impurity type.
6. (Original) The method of Claim 5, wherein the element of the first impurity type comprises phosphorus and/or arsenic.
7. (Original) The method of Claim 1, wherein doping the exposed silicon-based region with a gas containing an element of the first impurity type and forming a contact plug in the contact hole are performed in a chamber of the same manufacturing apparatus in-situ.

8. (Original) The method of Claim 3, wherein doping the exposed silicon-based region with a gas containing an element of the first impurity type is performed at a temperature of from about 400 to about 800 °C.

9. Cancelled.

10. (Original) The method of Claim 3, wherein doping the exposed silicon-based region with a gas containing an element of the first impurity type is performed for from about 30 to about 180 seconds.

11. (Currently Amended) The method of Claim 1, wherein patterning an interlayer dielectric of the semiconductor device to form a contact hole that exposes a silicon-based region of a first impurity type comprises patterning an interlayer dielectric of the semiconductor device to form a contact hole that exposes ~~silicon-based region of a first impurity type the silicon-based region comprises a region of a silicon substrate doped with the first impurity type.~~

12. (Currently Amended) The method of Claim 1, wherein ~~the silicon-based region comprises patterning an interlayer dielectric of the semiconductor device to form a contact hole comprises patterning an interlayer dielectric of the semiconductor device to form a contact hole that exposes a first silicon-based contact plug of a first impurity type and wherein doping the exposed silicon-based region comprises doping the exposed silicon-based contact plug with a gas containing an element of the first impurity type under a chamber pressure of from about  $6 \times 10^{-2}$  to about  $6 \times 10^{-4}$  Torr.~~

13. (Currently Amended) The method of Claim 12, wherein patterning an interlayer dielectric of the semiconductor device to form a contact hole that exposes a first silicon-based contact plug of a first impurity type the silicon-based region comprises patterning an interlayer dielectric of the semiconductor device to form a contact hole that exposes a polysilicon contact plug doped with the first impurity type.

14. (Original) The method of Claim 1, further comprising:  
forming a diffusion layer of the first impurity type in a semiconductor substrate of a second impurity type;  
depositing an interlayer dielectric on a surface of the semiconductor substrate where the diffusion layer of the first impurity type is formed; and  
wherein patterning an interlayer dielectric of the semiconductor device to form a contact hole that exposes a silicon-based region of a first impurity type comprises patterning the interlayer dielectric to form a contact hole that exposes the diffusion layer of the first impurity type as the exposed silicon-based region.

15. (Original) The method of Claim 1, further comprising:  
forming a diffusion layer of the first impurity type in a semiconductor substrate of a second impurity type;  
depositing a first interlayer dielectric on a surface of the semiconductor substrate where the diffusion layer of the first impurity type is formed;  
forming a first contact hole in the first interlayer dielectric to expose the diffusion layer of the first impurity type;  
forming a first contact plug in the first contact hole using a doped polysilicon;  
depositing a second interlayer dielectric on a surface of the semiconductor substrate where the first contact plug is formed;  
wherein patterning an interlayer dielectric of the semiconductor device to form a contact hole that exposes a silicon-based region of a first impurity type comprises patterning the second interlayer dielectric to form a second contact hole that exposes the first contact plug as the exposed silicon-based region.

16.-20. Cancelled.